

WEST Search History

DATE: Tuesday, February 08, 2005

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		<i>DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>	
<input type="checkbox"/>	L10	L8 same video	1
<input type="checkbox"/>	L9	L8 same display\$4	6
<input type="checkbox"/>	L8	L7 same (second near2 (information or data or content))	80
<input type="checkbox"/>	L7	L6 same (first near2 (information or content or data))	202
<input type="checkbox"/>	L6	compar\$4 same ((adjust\$4 or alter\$4 or chang\$4 or switch\$4 or modif\$9) near3 (rate or speed))	39546
<input type="checkbox"/>	L5	l1 same ((adjust\$4 or alter\$4 or chang\$4 or switch\$4 or modif\$9) near3 (rate or speed))	4
<input type="checkbox"/>	L4	l1 and ((adjust\$4 or alter\$4 or chang\$4 or switch\$4 or modif\$9) near3 (rate or speed))	126
<input type="checkbox"/>	L3	L2 and ((adjust\$4 or alter\$4 or chang\$4 or switch\$4 or modif\$9) near3 (rate or speed))	0
<input type="checkbox"/>	L2	(first adj display adj content) same (second adj display adj content)	10
<input type="checkbox"/>	L1	(compar\$4 near3 display near3 (output or content))	1265

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		<i>DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>	
<input type="checkbox"/>	L12	L11 same ((based or respons\$4 or depend\$4) near5 compar\$4)	9
<input type="checkbox"/>	L11	(chang\$4 or modif\$9 or switch\$4 or alter\$4) near5 (frame near2 rate)	1558
<input type="checkbox"/>	L10	L8 same video	1
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L12: Entry 7 of 9

File: USPT

Aug 8, 1995

DOCUMENT-IDENTIFIER: US 5440685 A

**** See image for Certificate of Correction ****

TITLE: Apparatus and method for controlling manipulation and storage of image data

Detailed Description Text (12):

Referring to FIG. 6, the storage condition control section 110 comprises the frame rate comparator 111 and the media selector 112. The frame rate comparator 111 compares the inherent frame rate indicated by the performance value with the set frame rate set in the manipulation size setting unit 60. An output of the frame rate comparator 111 is supplied to the media selector 112. The media selector 112 selects a medium where the image data should be stored in response to the comparison result supplied to the frame rate comparator 111. The media selector 112 is connected to the free capacity determining unit 106, a frame rate changing unit 113 and a mask region changing unit 114.

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L12: Entry 5 of 9

File: USPT

Aug 22, 2000

DOCUMENT-IDENTIFIER: US 6106467 A

TITLE: Apparatus for ultrasonic diagnosis with variable frame rate

Detailed Description Text (3):

The focusing controller 11 serves to control the transmission-reception control circuit 2 to thereby set the number of focusing steps and the focusing position. The action for increasing or decreasing the number of focusing steps is carried out in response to signals received from a frame rate comparator 13 (to be described below). The focusing controller 11 also serves to respond to the size switching signal from the size changer 10 by transmitting to the frame rate calculator 12 a signal indicative of

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May 15, 2001

TITLE: Signal to noise estimation of forward link traffic channel for fast power control

The two estimated quality metrics are then used to generate two different power control bit streams. The power control bits are based on the comparison of the two estimated quality metrics with a predetermined threshold, ($\sup E$ b/N.sub.o).sub.setpoint. One power control bit stream is generated under the assumption that the frame rate has not changed while the other power control bit stream is generated under the assumption that the frame rate has changed. These power control bit streams are transmitted to the base station.

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Apr 23, 2002

TITLE: Mobile phone with communication channel switching determinating unit

The channel switching control section may determine a frame error rate threshold value based on the past channel switching result, and compare the detected frame error rate and the determined frame error rate threshold value. Then, the channel switching control section may determine that the communication quality is degraded when the detected frame error rate is equal to or larger than the determined frame error rate threshold value. In this case, the channel switching control section may set a first threshold value as the determined frame error rate threshold value, when the past channel switching result indicates that a success rate of past channel switching operations is equal to or higher than a success rate threshold value. Also, the channel switching control section may set a second threshold value as the determined frame error rate threshold value when the past channel switching result indicates that the success rate of the past channel switching operations is lower than the success rate threshold value. Here, the second threshold value is larger than the first threshold value. The past channel switching operations may be hand-over operations, or intra-station channel switching operations.

2. A mobile phone according to claim 1, wherein said channel switching control section determines a frame error rate threshold value based on said past channel switching result, compares said detected frame error rate and said determined frame error rate threshold value, and determines that the communication quality is degraded when said detected frame error rate is equal to or larger than said determined frame error rate threshold value.

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Jan 21, 2003

TITLE: Channel switching device and channel switching method

1. A channel switching apparatus comprising: a desired wave reception electric field strength detecting section that detects a desired wave reception electric field strength of a mobile station; an interference wave reception electric field strength detecting section that detects an interference wave reception electric field strength at a same frequency; a comparing section that compares said an output of said detecting sections with each other; a frame error rate detecting section that detects an error rate in a receiving signal; and a switching section that compares a comparison result of said comparing section with a detection result of said frame error rate detecting section and switches a communication channel based on said comparison result of said comparing section and said detection result of said frame error rate detecting section.

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L12: Entry 1 of 9

File: USPT

Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6661846 B1

TITLE: Adaptive clocking mechanism for digital video decoder

CLAIMS:

14. An apparatus for modifying a frame rate, comprising: means for receiving a reference clock frequency and a video frame rate from a video bit-stream; means for selecting a modifier based on a comparison of the received video frame rate and an expected video frame rate, said modifier being 1001/1000, 1/1, or 1000/1001; and means for producing a reference clock by multiplying said reference frequency by said selected modifier, in order to adjust a frame rate at which said video bit-stream is decoded.

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L10: Entry 1 of 1

File: USPT

Mar 27, 1984

DOCUMENT-IDENTIFIER: US 4439765 A

TITLE: Radar video processor

Detailed Description Text (4):

The scan-to-scan correlator 26 and adaptive noise thresholder 24 are coupled to the changing video transmitter 27. The scan-to-scan correlator 26 and changing video transmitter 27 comprise comparison circuitry which transmits the present video when it is substantially different from the time-averaged video. The changing video transmitter 27 is in essence a subtraction circuit which subtracts the smooth video signals provided by the scan-to-scan correlator 26 from the present video signals provided by the adaptive noise thresholder 24. The changing video transmitter 27 transmits only those present video signals which differ from the signals provided by the scan-to-scan correlator 26 by a predetermined amount. Hence, the changing video transmitter 27 transmits only moving targets or video signals which change in amplitude from scan to scan through the data link 31. The changing video transmitter is coupled to the first data link buffer 30 and hence through the data link 31 to the second data link buffer 32. The second data link buffer 32 is then coupled to a radar display 34, such as a PPI display, or the like, which allows the output signals from the changing video transmitter 27 to be applied to the radar display 34. The first buffer 30 is used to provide temporary storage of the data, to format the data, and change the data transmission rate from a real time, high speed radar data rate to a low speed, data link data transmission rate. The second buffer 32 provides a similar set of functions to interface the data link 31 with the digital memory 33 and radar display 34. The digital memory 33 is also coupled to the radar display 34 which allows the radar clutter signals stored therein to be applied to the radar display 34 at the option of the radar system operator. It is to be understood that the radar display 34 is normally located at a point remote from the antenna and signal processor, typically from 10-200 miles, which necessitates the use of the data link 31.

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L9: Entry 1 of 6

File: USPT

Dec 12, 2000

DOCUMENT-IDENTIFIER: US 6160532 A

TITLE: Digital gamma correction circuit, gamma correction method, and a liquid crystal display apparatus and electronic device using said digital gamma correction circuit and gamma correction method

Brief Summary Text (30):

The invention according to claim 15 can thus read the correction data from an applied voltage-transmittance curve for the liquid crystal display panel to enable gamma correction when gradation of the input image data is low and the image data is associated with the first range, and when gradation of the input image data is high and the image data is associated with the second range. High precision gamma correction can therefore be achieved in the first and second ranges even when the rate of change in the applied voltage-transmittance characteristic of the liquid crystal display panel is varied. In addition, gamma correction based on a linear approximation is applied in the third range between the first and second ranges because the rate of change in the applied voltage-transmittance characteristic of the liquid crystal display panel is substantially constant. Therefore, the capacity of the memory table can be reduced when compared with gamma correction of the full gradation range using only a memory table.

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L5: Entry 1 of 4

File: USPT

Jun 15, 2004

DOCUMENT-IDENTIFIER: US 6750837 B1

TITLE: Ferroelectric liquid crystal display

Detailed Description Text (16):

Further, the length of black display can be adjusted by adjusting the length of the reset period automatically. FIG. 7 is a block diagram showing a circuit configuration for adjusting the length of the reset period automatically. This circuit configuration includes display data memories 21a, 21b for storing the display data from the display data generating circuit 21 of FIG. 6 and a display data comparison circuit 21c for comparing the display data of the display data memories and outputting the result to the driving voltage waveform control circuit 22 of FIG. 6. In this circuit configuration, the display data of the successive screens from the display data generating circuit 21 are stored in the display data memories 21a, 21b, and the two stored display data are compared in the display data comparison circuit 21c. In the case where the change rate of the data thus compared is large, it is determined that an image having a rapid motion is on display. In the case where the change rate of the data compared is small or zero, on the other hand, it is determined that an image having a slow motion or a still image is on display, and the result is input to the driving voltage waveform control circuit 22. In the case where the change rate of the data compared is large, the reset period is automatically lengthened. In the case where the change rate is zero or substantially nil, on the other hand, the reset period is shortened automatically. Also in this case, the brightness of the backlight is changed by the backlight control circuit 26 in accordance with the length of the reset period. Incidentally, the backlight control circuit 26 changes the brightness of the backlight in accordance with the output of the display data comparison circuit 21c.

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